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Gloster, C., Jr.; Subramanian, S.;
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 Pages:366 - 369

[\[Abstract\]](#) [\[PDF Full-Text \(264 KB\)\]](#) IEEE CNF**2 A novel scan architecture for power-efficient, rapid test [sequential circuits]**

Sinanoglu, O.; Orailoglu, A.;
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 Pages:299 - 303

[\[Abstract\]](#) [\[PDF Full-Text \(450 KB\)\]](#) IEEE CNF**3 Static test compaction for full-scan circuits based on combinational test sets and non-scan sequential test sequences**

Pomeranz, I.; Reddy, S.M.;
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[\[Abstract\]](#) [\[PDF Full-Text \(247 KB\)\]](#) IEEE CNF**4 Reducing test power during test using programmable scan chain disable**

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